AMENDMENT(S) TO THE SPECIFICATION:

Kindly amend paragraph [0060] on page 12 as follows:

--[0060] Note that while in one embodiment, the address indicates to the DMA controller 307 whether a DMA transfer is to or from the DMA engine 324 or the memory ~~interface313,~~ interface 313, in an alternate embodiment, a separate indication, e.g., a control bit is used to indicate whether a DMA transfer is to or from the DMA engine 324 or the memory ~~interface313.~~ interface 313.

Kindly amend paragraph [0064] on page 12 as follows:

--[0064] Consider first the operation during transmit of the embodiment shown in FIG. 2. In this case, the switch 229 routes any ~~packet~~ packets that are for transmission by the wireless station 200 to the wireless station. Such packets are queued in the host processing system, e.g., in the host memory 2315, and the host communicates with the lower MAC 203 to set up DMA transfers of data in the host memory, as required, e.g., by communicating the packet headers and the set of buffer descriptors (the buffer descriptor chain) for each packet.--

Kindly amend paragraph [0073] on page 14 as follows:

--[0073] The network DMA engine 324 interprets the information in the second special-type packets, i.e., in the streaming data encapsulating packets. One aspect is that the pointer and length information in the second-type-special packets is used to match the packet as a response to a DMA request. The network DMA engine 324 removes the data and communicates them via the bus 309 as responses to the matching DMA requests. To the host system bus, these appear as regular DMA responses transfers set up by the host DMA controller 307, since for such transfers, the network DMA ~~engine 328~~ engine 324 is set up as if it was a memory interface.

Kindly amend paragraph [0085] on page 17 as follows:

--[0085] The DMA request from the host DMA controller 307 is translated by the network DMA engine 324 to a packet of the second special type that includes the pointer and length data for the transfer, and the data element of the transfer to be written into the switch memory. The packet of the second type is sent to the switch 329 via the network via the Ethernet MAC and PHY interface and the network ~~link 327.~~ link 328.--

Kindly amend paragraph [0086] on page 17 as follows:

--[0086] At the switch, the packet of the second type is received by the Ethernet MAC and PHY interface 336 that includes a filter 337 that filters out the packet of the second type and passes the information therein, including the data, to the network DMA engine ~~338.~~ 338. The network DMA engine 338 interprets the request and sets up for, and writes the data to the memory location in the switch memory 335.--